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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2827
Examiner: David GRAYBILL

In Re PATENT APPLICATION Of:

Applicants : Mitsuru KOMIYAMA

Serial No. : 09/963,590

Filed : September 27, 2001

For : MULTI-CHIP PACKAGE TYPE SEMICONDUCTOR DEVICE

Attorney Ref. : F00ED0023

AMENDMENT

June 17, 2002

Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is submitted with the applicant's Request for Continued Examination pursuant to 37 C.F.R. §1.114(a). Please amend the above-identified application as follows:

IN THE CLAIMS:

13 (amended). A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first terminal pad and a conductive relay pad, the conductive relay pad including a first area and a second area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to the conductive relay pad in the second area;

a first internal terminal connected to the first terminal pad; and

a second internal terminal connected to the conductive relay pad in the first area.

-- 19 (new). A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

20 (new). A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first conductive portion and a second conductive portion, the second conductive portion having a first area and a second area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to the second conductive portion in the first area;

A2 cont

a first internal terminal connected to the first conductive portion; and

a second internal terminal connected to the second conductive portion in the second area.

21 (new). A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

22 (new). A multi-chip package type semiconductor device, as claimed in

claim 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

23 (new). A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are spaced from each other.

24 (new). A multi-chip package type semiconductor device, as claimed in claim 20, further comprising:

a bump formed on the second conductive portion in the second area; and

a first wire, the first wire having one end connected to the second terminal and the other end connected to the bump.

25 (new). A multi-chip package type semiconductor device, comprising:

an insulating substrate;

a first conductive pattern formed on the insulating substrate;

a first semiconductor chip mounted on the insulating substrate;

a second conductive pattern formed on the first semiconductor chip, the second conductive pattern having a first area and a second area;

a second semiconductor chip mounted on the first semiconductor chip;

a third conductive pattern formed on the second semiconductor chip;

a first wire connected between the first area of the second conductive pattern and the third conductive pattern; and

a second wire connected between the second area of the second conductive pattern and the first conductive pattern.

26 (new). A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second area are located along the side of the first semiconductor chip.

27 (new). A multi-chip package type semiconductor device, as claimed in claim 25, further comprising:

a first bump formed on the first area of the second conductive pattern; and

a second bump formed on the third conductive pattern,

wherein the first wire is connected to the first area through the first bump and the second wire is connected to the third conductive pattern through the second bump.

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28 (new). A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second area are spaced each other. --

REMARKS

The Notice of Allowance of April 10, 2002 has been received. Claim 13 has been amended, and new claims 19-28 have been added. Therefore, claims 1-28 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

Initially, it is noted that this Amendment increases the total number of claims

pending in the application to twenty-eight (28) from eighteen (18), thus requiring an excess claim fee of $144.00 for four claims in excess of twenty. It is further noted that this Amendment increases the total number of independent claims pending in the application to five (5) from three (3), thus requiring an excess independent claim fee of $168.00 for two claims in excess of three. Please charge the necessary fee of $312.00 to our Deposit Account No. 50-0945.

Allowed claims 1-12, and 14-18 are not amended. Thus, the condition of allowing claims 1-12, and 14-18 should be maintained. Claim 13 is amended merely to correct a typographical error. Thus, this amendment does not narrow the scope of claim 13.

In view of the foregoing, claims 1-18 are maintained to be allowable. Examination of new claims 19-18 is respectfully requested. Should any fee be further needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Attached hereto is a marked-up version of the changes made to claim by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted

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